

ESD Services

Synopsys TCAD Services

Overview

Electrostatic discharge (ESD) is a major threat for integrated circuit (IC) reliability. TCAD device simulation can identify and investigate ESD-relevant effects and the internal behavior of the device under ESD stress conditions, which are not generally accessible by measurement. In particular, TCAD can be successfully used to study 3D effects arising from device layout or inhomogeneous current (see Figure 1).

Synopsys offers two TCAD-based modeling services: TCAD ESD Workbench and ESD Circuit Compact Model Development. They are aimed to reduce IC and device design-cycle time and to make ‘first silicon success’ possible, thereby ensuring competitiveness of products in the market. The experienced Synopsys TCAD Services group provides reliable modeling of devices and circuits under ESD stress conditions based on a strong track record in this field.

Introduction

The operational regime of devices under ESD stress is far outside the range of normal operational conditions. Among the most important physical effects in ESD are self-heating, conductivity modulation due to high carrier injection, nonuniform operation (current filamentation), and avalanche breakdown at reverse-biased junctions. TCAD device simulation is a valuable tool for investigating these effects, which often can replace or, at least, complement expensive measurements.

With transmission line pulse (TLP) characterization, device characteristics up to very high current levels can be obtained

while preventing early destruction due to self-heating. In device simulation, TLP is used to calibrate the high-current and high-temperature regime to measurements. For qualification and specification of ESD robustness, we can model human body model (HBM), machine model (MM), and charged device model (CDM) stress conditions.

The basic functionality of an ESD protection device or ESD protection circuit consists of providing a low-resistivity discharge current path, which prevents the internal circuitry and the protection device or circuit itself from being damaged during an ESD event, while remaining ‘transparent’ to the internal

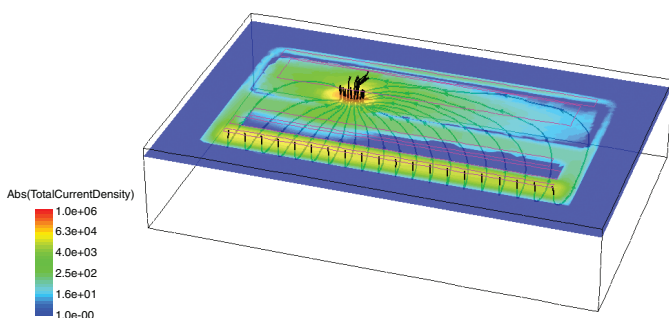


Figure 1: Formation of current filament leading to temperature hot spot in a device during an ESD pulse using Sentaurus Device 3D device simulation.

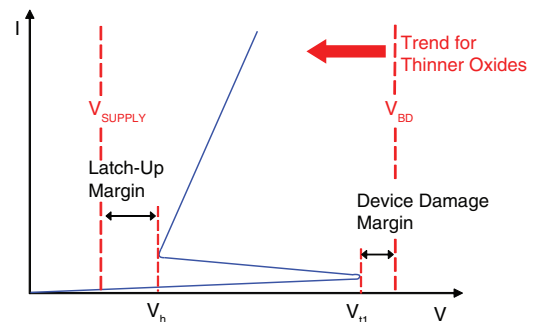


Figure 2: Typical ESD design window for protection devices.

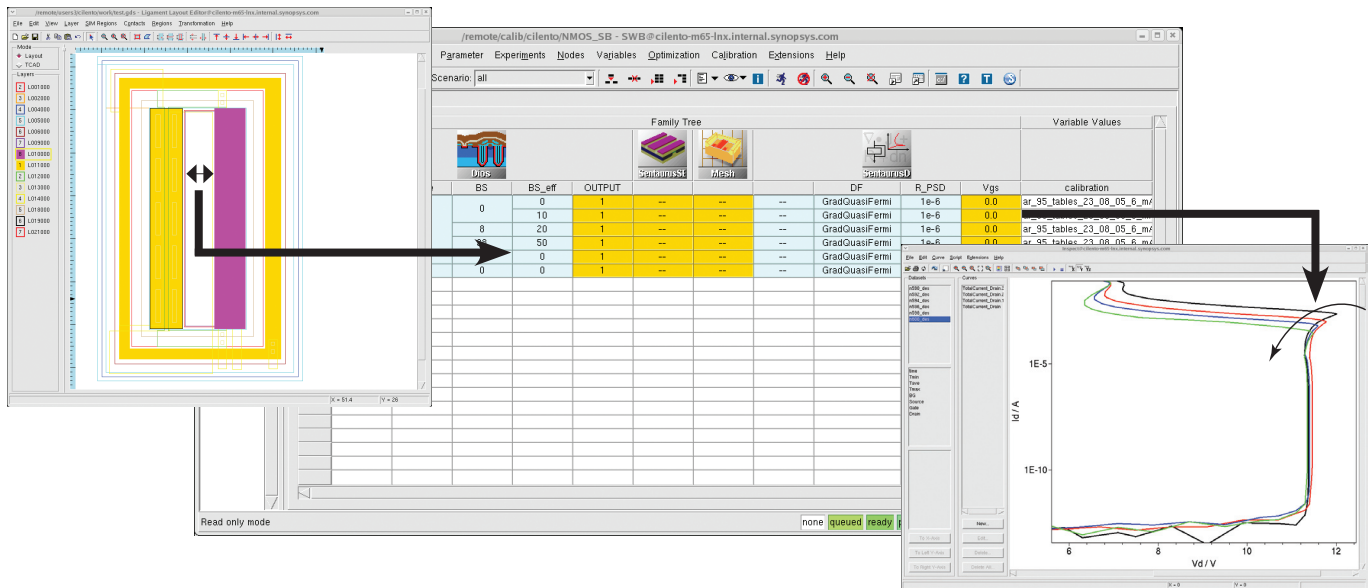


Figure 3: Simulation flow embedded in Sentaurus Workbench showing the influence of layout variations on the electrical characteristics.

circuitry under normal operation conditions. Figure 2 shows the most important parameters of the so-called ESD design window.

TCAD ESD Workbench

Establishing a full-fledged ESD TCAD workbench from process and layout information, and from the calibration of simulation models including high current/high temperature regime, allows the evaluation of process variation influences, the determination of layout dependency, and the optimization of ESD structures. The improved understanding of internal device failure modes leads to optimized input/output protection structures and the possibility of virtual testing and development of new structures. The service, which targets device engineers and TCAD teams, speeds up ESD design to keep pace with IC developments at reduced design-cycle times by reducing time-to-market and cost-to-market.

The starting point for a successful calibration of the ESD characteristics of a device is a well-calibrated, low-current and breakdown process and device simulation model set. In a further step, ESD-related modeling is addressed by:

High-Temperature Calibrated Models

- Impact ionization
- Mobility (low-field, carrier-to-carrier scattering, high-field saturation)

Bipolar-specific Models (Snapback Phenomena)

- Bandgap narrowing
- Recombination

Electrothermal Effects

- Self-heating mechanisms and heat flows

Information About Layout and Measurement Setup

- Three-dimensional layout features
- Contact resistances

At the end, the goal is to obtain one set of parameters that allow the predictive simulation of ESD behavior and, at the same time, can be used for normal operation conditions.

Deliverables to Customers

- Simulation setups, projects, and results embedded in Sentaurus Workbench (see Figure 3)
- Calibrated parameter set
- Optional: Investigation of ESD-related effects (2D and 3D)
- Comprehensive report
- On-site review, training, and methodology transfer

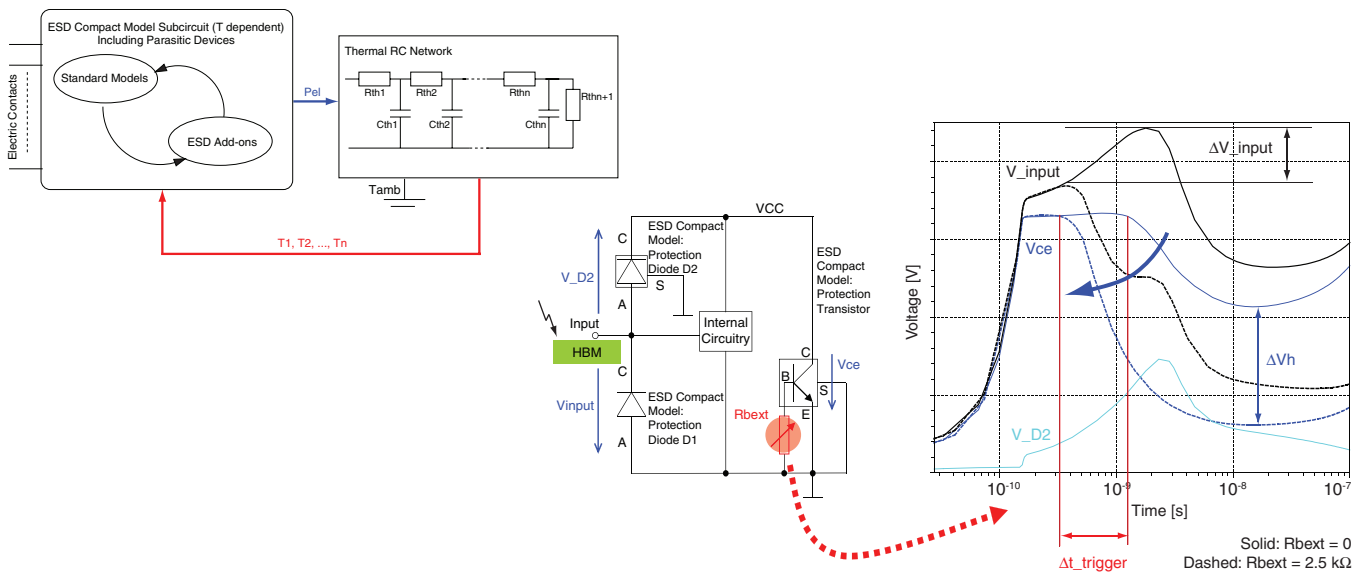


Figure 4: (Left) Modular setup of ESD compact models including thermal network fed by dissipated power P_{el} and (right) an ESD compact model application within a simple input pad protection circuit showing the tuning of the trigger behavior of the protection transistor.

ESD Circuit Compact Model Development

There is a strong need to include ESD compact models in circuit simulations to predict critical current paths and critical node values, and to enhance input/output design quality.

The insight gained by TCAD allows the development of physically based compact model add-ons for ESD. Internal device characteristics not accessible by measurements can be used to obtain these add-ons.

Calibrated process and device simulation enables parameter extraction for ESD compact models, avoiding expensive, noisy, and destructive measurements.

To keep the compact model development effort to a reasonable level, a modular modeling strategy is chosen. This strategy is often referred to as *macro-modeling* or *subcircuit modeling* in the literature. We retain the standard model of the corresponding device (for example, a Gummel–Poon or BSIM model) for normal operation conditions and extend it by ESD-specific add-on modules to form a full ESD compact model.

The operational regime of devices under ESD stress is beyond the range in which the standard compact models have been tested and verified; whereas, the full ESD compact models allow for reproducing behavior under ESD stress in circuit simulation. Thermal effects are included by establishing a feedback loop between electric and thermal domains. Figure 4 shows how the ESD compact models are set up as well as a simple application.

The calibrated ESD compact models can be used within circuit simulations to determine critical current paths, to identify endangered devices, and to optimize protection circuitry. Circuit simulations with up to 15 ESD compact models and approximately 100 standard models are feasible. The limitation arises from the well-known convergence problems caused by the strong nonlinear behavior of the protection devices under ESD stress conditions and from their interaction with the rest of the circuit. These nonlinearities cannot be eliminated, but they can be reduced to an acceptable level by paying particular attention to numeric issues. While the nonlinear behavior (for example, snapback devices) is one key issue to account for in ESD simulations, it makes the numeric treatment extremely unstable and computing intensive. Nevertheless, the circuit complexity goes beyond simple input/output pad protection configurations, including large parts of the internal circuit. For the implementation of the ESD add-on model equations, Verilog-A behavioral modeling language can be used. Verilog-A can be read by most common circuit simulators such as HSPICE®.

Deliverables to Customers

- TCAD workbench embedded in Sentaurus Workbench
- ESD compact models
- Compact model parameters and extraction methodology
- Optional: Optimization of protection circuits
- Comprehensive report
- On-site review, training, and methodology transfer

Table 1: ESD experience: Research projects.

Project	Project Tasks	Technology	Devices
SIDRA*	CDM device and circuit simulation methodology	Submicron CMOS, smart power	NMOS, diodes, SCRs
DEMAND*	Mobility and impact ionization model improved up to 1000 K and 700 K, respectively	Smart power	DMOS, BJT
ESDEM*	New set of high-temperature models	Submicron CMOS, smart power	NMOS, LDMOS
Cooperation Synopsys–ETH Zurich	ESD TCAD methodology, ESD compact modeling, high-temperature measurements, ESD for optoelectronics	Submicron CMOS, smart power	NMOS, DMOS, diodes, SCRs

* European research project.

Table 2: ESD experience: Commercial projects.

Project	Project Tasks	Technology	Devices
Project 1	Process, device, and ESD calibration, device robustness evaluation with respect to HBM, device robustness optimization	BCD	LV MOS, BJT, LDMOS
Project 2	Layout optimization (3D)	BCD	NPN
Project 3	Process, device, and ESD calibration, compact model development, parameter extraction methodology, ESD circuit simulations	BCD	Three BJTs, two diodes, resistor
Project 4	Contact size optimization (3D) with respect to hot-spot temperature, and breakdown and snapback voltage	Smart power	NLDMOS

Experience and Track Record

Our broad experience in the ESD field includes various BiCMOS and BCD/smart power process and device calibrations, ranging from commercial to research projects.

For more information about Synopsys TCAD products and services, go to <http://www.synopsys.com/Tools/Pages/default.aspx>, or contact your local Synopsys representative, or email tcad_team@synopsys.com.



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